In The Claims:

1. (Currently Amended) An apparatus for performing a data encryption operation in an electronic system, comprising:

a processor coupled to said electronic system [[for]], said processor creating an encryption structure in a memory device, said processor also selectively programming control registers ~~to thereby facilitate efficiently performing~~ to perform said data encryption operation;

a DMA engine coupled to said processor [[for]], said DMA engine accessing said encryption structure and said control registers ~~to thereby control said data encryption operation; and~~, said DMA engine including an encryption module ~~coupled to said DMA engine~~ that utilizes command information from said encryption structure and control information from said control ~~registers for processing~~ to process source data to produce destination data during said data encryption operation.

2. (Original) The apparatus of claim 1 wherein said data encryption operation includes at least one of a data encryption process and a data decryption process.

3. (Original) The apparatus of claim 2 wherein said memory device receives said source data from a source entity coupled to said electronic system, said memory device responsively storing said source data into a source data memory location until said encryption module requires said source data to perform said data encryption operation.

4. (Original) The apparatus of claim 2 wherein said electronic system is implemented as one of an audio/visual electronic device, a consumer electronics device, a portable electronics device, and a computer device.

5. (Original) The apparatus of claim 2 wherein said electronic system includes a bridge device that facilitates bi-directional communications between said processor, one or more peripheral devices, said DMA engine, said encryption module, and said memory device.

6. (Original) The apparatus of claim 5 wherein said bridge device includes a processor interface for communicating with said processor, a memory interface for communicating with said memory device, and one or more peripheral interfaces for communicating with said one or more peripheral devices.

7. (Original) The apparatus of claim 2 wherein said encryption structure includes at least one command structure that has command information for performing said data encryption operation.

8. (Original) The apparatus of claim 7 wherein said command structure includes a starting source address, a starting destination address, a transfer-bytes total field, a next command-structure pointer, and a control status command.

9. (Original) The apparatus of claim 8 wherein said control status command includes an encryption/decryption field to indicate whether to perform one of said encryption process and said decryption process, an enabled/disabled field to indicate whether said data encryption operation is currently enabled, an interrupt field to designate whether an interrupt should occur following said data encryption operation, a last command field to indicate a final command structure in a linked list, and a transfer path identifier to indicate a source entity for said source data and a destination entity for destination data.

10. (Original) The apparatus of claim 2 wherein said encryption structure includes a series of command structures that are linked together in a linked list to thereby perform a series of data encryption operations.

11. (Original) The apparatus of claim 2 wherein said DMA engine includes a state machine for controlling said data encryption operation, one or more command registers for locally storing one or more command structures from said encryption structure, said control registers, a data buffer, an encryption key register, and said encryption module.

12. (Original) The apparatus of claim 2 wherein said control registers include a start register that said processor may program to start said data encryption operation, a halt/resume register that said processor may program to halt or resume said data encryption operation, a clear interrupt register that said processor may program to clear an interrupt of said data encryption operation, a link list address register that said processor may program with a physical address in said memory device of a first command structure in said encryption structure, and a status register that said DMA engine may program to indicate a current status of said data encryption operation.

13. (Original) The apparatus of claim 2 wherein said processor initially creates said encryption structure in said memory device, said encryption structure including one or more command structures that each include command information for performing a separate data encryption operation.

14. (Original) The apparatus of claim 13 wherein said processor programs said control registers with data encryption information that is then locally available to said DMA engine for performing said data encryption operation.

15. (Original) The apparatus of claim 14 wherein said processor instructs said DMA engine to perform said data encryption operation after programming said control registers, said processor then releasing control of said data encryption operation and performing other system processing tasks for said electronic system.

16. (Original) The apparatus of claim 15 wherein said DMA engine copies one or more designated command structures from said encryption structure in said memory device into one or more command registers that are locally coupled to said DMA engine.

17. (Original) The apparatus of claim 16 wherein said DMA engine controls said data encryption operation by referring to said control registers and said command registers.

18. (Original) The apparatus of claim 17 wherein a state machine coupled to said DMA engine transfers said source data from said memory device to a data buffer coupled to said encryption module, said encryption module responsively performing at least one of said data encryption process and said data decryption process to produce said destination data, said state machine then storing said destination data back into said memory device.

19. (Original) The apparatus of claim 18 wherein said DMA engine detects a completion condition while performing said data encryption operation, said DMA engine responsively notifying said processor regarding said completion condition.

20. (Original) The apparatus of claim 19 wherein said processor transfers said destination data from said memory device to a destination entity that is coupled to said electronic system.

21. (Currently Amended) A method for performing a data encryption operation in an electronic system, comprising ~~the steps of~~:

creating an encryption structure in a memory device by utilizing a processor;

programming control registers ~~with~~ by said processor ~~to thereby facilitate efficiently performing~~ to perform said data encryption operation;

accessing said encryption structure and said control registers with a DMA engine ~~to thereby control said data encryption operation~~; and

processing source data with an encryption module of said DMA engine to produce destination data, said encryption module utilizing command information from said encryption structure and control information from said control registers to perform said data encryption operation.

22. (Original) The method of claim 21 wherein said data encryption operation includes at least one of a data encryption process and a data decryption process.

23. (Original) The method of claim 22 wherein said memory device receives said source data from a source entity coupled to said electronic system, said memory device responsively storing said source data into a source data memory location until said encryption module requires said source data to perform said data encryption operation.

24. (Original) The method of claim 22 wherein said electronic system is implemented as one of an audio/visual electronic device, a consumer electronics device, a portable electronics device, and a computer device.

25. (Original) The method of claim 22 wherein said electronic system includes a bridge device that facilitates bi-directional communications between said processor, one or more peripheral devices, said DMA engine, said encryption module, and said memory device.

26. (Original) The method of claim 25 wherein said bridge device includes a processor interface for communicating with said processor, a memory interface for communicating with said memory device, and one or more peripheral interfaces for communicating with said one or more peripheral devices.

27. (Original) The method of claim 22 wherein said encryption structure includes at least one command structure that has command information for performing said data encryption operation.

28. (Original) The method of claim 27 wherein said command structure includes a starting source address, a starting destination address, a transfer-bytes total field, a next command-structure pointer, and a control status command.

29. (Original) The method of claim 28 wherein said control status command includes an encryption/decryption field to indicate whether to perform one of said encryption process and said decryption process, an enabled/disabled field to indicate whether said data encryption operation is currently enabled, an interrupt field to designate whether an interrupt should occur following said data encryption operation, a last command field to indicate a final command structure in a linked list, and a transfer path identifier to indicate a source entity for said source data and a destination entity for destination data.

30. (Original) The method of claim 22 wherein said encryption structure includes a series of command structures that are linked together in a linked list to thereby perform a series of data encryption operations.

31. (Original) The method of claim 22 wherein said DMA engine includes a state machine for controlling said data encryption operation, one or more command registers for locally storing one or more command structures from said encryption structure, said control registers, a data buffer, an encryption key register, and said encryption module.

32. (Original) The method of claim 22 wherein said control registers include a start register that said processor may program to start said data encryption operation, a halt/resume register that said processor may program to halt or resume said data encryption operation, a clear interrupt register that said processor may program to clear an interrupt of said data encryption operation, a link list address register that said processor may program with a physical address in said memory device of a first command structure in said encryption structure, and a status register that said DMA engine may program to indicate a current status of said data encryption operation.

33. (Original) The method of claim 22 wherein said processor initially creates said encryption structure in said memory device, said encryption structure including one or more command structures that each include command information for performing a separate data encryption operation.

34. (Original) The method of claim 33 wherein said processor programs said control registers with data encryption information that is then locally available to said DMA engine for performing said data encryption operation.

35. (Original) The method of claim 34 wherein said processor instructs said DMA engine to perform said data encryption operation after programming said control registers, said processor then releasing control of said data encryption operation and performing other system processing tasks for said electronic system.

36. (Original) The method of claim 35 wherein said DMA engine copies one or more designated command structures from said encryption structure in said memory device into one or more command registers that are locally coupled to said DMA engine.

37. (Original) The method of claim 36 wherein said DMA engine controls said data encryption operation by referring to said control registers and said command registers.

38. (Original) The method of claim 37 wherein a state machine coupled to said DMA engine transfers said source data from said memory device to a data buffer coupled to said encryption module, said encryption module responsively performing at least one of said data encryption process and said data decryption process to produce said destination data, said state machine then storing said destination data back into said memory device.

39. (Original) The method of claim 38 wherein said DMA engine detects a completion condition while performing said data encryption operation, said DMA engine responsively notifying said processor regarding said completion condition.

40. (Original) The method of claim 39 wherein said processor transfers said destination data from said memory device to a destination entity that is coupled to said electronic system.

41. (Original) An apparatus for performing a data encryption operation in an electronic system, comprising:

means for creating an encryption structure in a memory device;

means for programming control registers to thereby facilitate efficiently performing said data encryption operation;

means for accessing said encryption structure and said control registers to thereby control said data encryption operation; and

means for processing source data to produce destination data during said data encryption operation.

42. (Original) An apparatus for performing a data processing operation in an electronic system, comprising:

a processor coupled to said electronic system for creating a data structure in a memory device, said processor also selectively programming control registers to thereby facilitate efficiently performing said data processing operation;

an engine coupled to said processor for accessing said data structure and said control registers to thereby control said data processing operation; and

a processing module coupled to said engine for processing source data to produce destination data during said data processing operation.